Coaxial Transceiver Interface

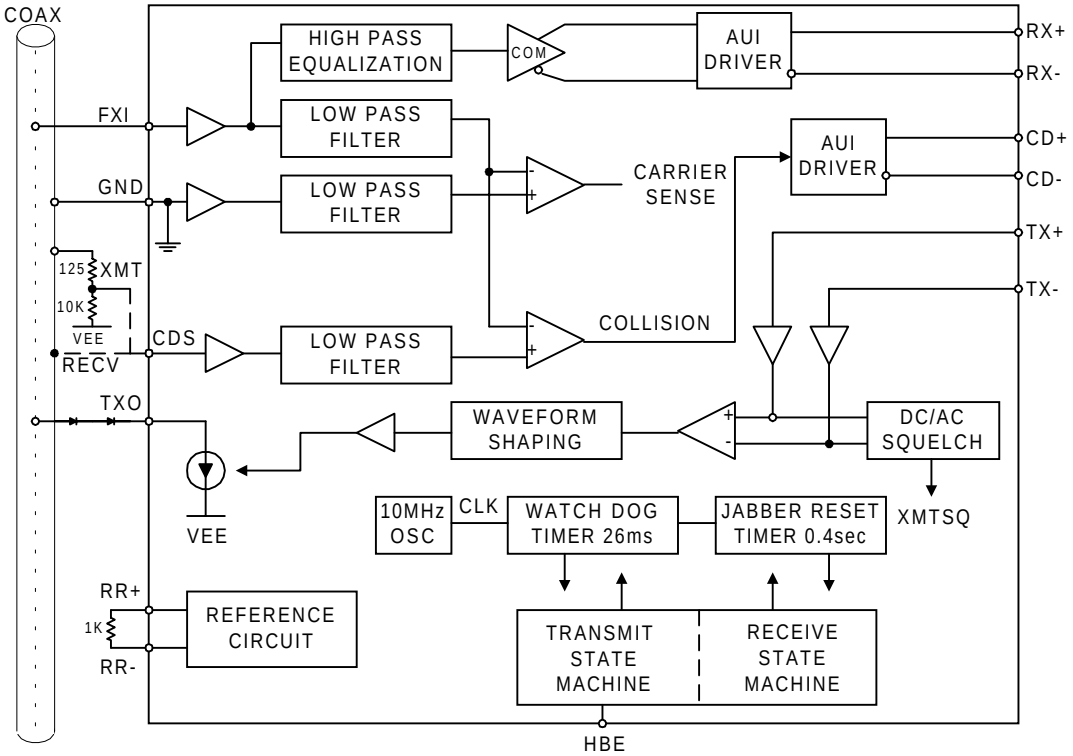
FEATURES

- Compatible with IEEE 802.3 10Base5 (Ethernet) and 10Base2 (Cheapernet).
- Internal AUI squelch circuitry for noise rejection.
- Transmission IDL detection at end of packet and dribble bit rejection window.
- Reception dribble bit rejection window.
- Reception and transmission mode collision detection.
- Extended collision detection to turn off receiving path.
- CD heartbeat externally controllable.
- Advanced low-power, high-performance CMOS technology.
- ESD protection greater than 2000 Volts.
- 16-pin PDIP and 28-pin PLCC packages.

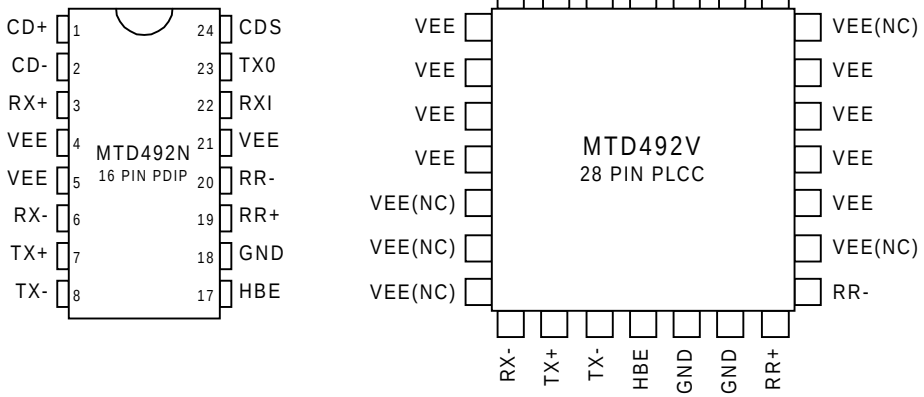
GENERAL DESCRIPTION

The MTD492 transceiver integrates the coaxial cable interface functions of the Medium Attachment Unit (MAU) in Ethernet or Cheapernet LAN applications. In an Ethernet 10Base5 network, MTD492 is mounted on the thick Ethernet coaxial cable and connects to a station through an AUI cable. For Cheapernet applications, MTD492 is connected to the Cheapernet coaxial cable through a BNC connector and is usually mounted on the LAN adapter in a station.

BLOCK DIAGRAM



1.0 CONNECTION DIAGRAM



2.0 PIN DESCRIPTIONS

Name	I/O	PDIP Pin#	PLCC Pin#	Description
TX+,TX-	I	7,8	13,14	**Transmission Data Input.** A balanced differential line receiver which receives inputs from the off-chip Manchester Code Converter(MCC) to the Transmitter. The common mode voltage on TX+ is set internally .
HBE	I	9	15	**Heartbeat Enabler.** The CD heartbeat test is enabled when HBE is connected to Ground and disabled when HBE is connected to VEE. This pin is internally biased at 0.5 VEE. Test mode is enabled if this pin is left floating or biased in the range of -3.5V to -5.5V. Jabber is disabled in test mode. Exiting the jabber disable mode requires at least jabber reset time.
RR+,RR-	I	11,12	18,19	**External Resistor.** A 1kΩ/1% resistor should be connected across these pins to correctly set internal operating currents. RR+ is internally shorted to GND.
RXI	I	14	26	**Network Receiving Input.** Should be connected to the COAX center conductor. Signals meeting receiver squelch limits are recovered and output on RX+. RXI also detects the collision voltage level.
CDS	I	16	1	**Collision Detection Sense.** Connects directly to the COAX shield, providing a reference for the collision detection voltage level for reception-mode detection. An external bias network can be used to shift the detection threshold for transmission-detection mode.
CD+,CD-	O	1,2	2,3	**Collision Output.** A balanced differential line driver drives this output pair from the collision detection circuitry. A 10MHz signal from the internal oscillator is transferred to these outputs in the event of collision, excessive transmission (jabber), or during heartbeat condition. These outputs are open sources, and pull-down resistors of 510Ω to VEE are required. To minimize power dissipation, both open source outputs are disabled during idle condition, allowing the common mode on the pull-down resistors to be pulled to VEE.

RX+,RX-	O	3,6	4,12	**Reception Data Output.** A balanced differential output drives the data recovered from the network to the MCC. These outputs are also open sources, and pull-down resistors of 510Ω to VEE are required. These pins are biased at -2V during idle time. When an extended period of collision condition happens, the receiving path is disabled. Any interruption of collision will re-enable the receiving path.
TXO	O	15	28	**Transmission Output.** Should be connected to the coaxial cable via either one (Cheapernet) or 2 serial isolation diodes (Ethernet).
GND		10	17	**Positive Supply Pin(Ground).** Should be connected to the COAX shield.
VEE		4,5, 13	5, 6, 7, 8, 9, 10, 11, 20, 21, 22, 23, 24, 25	**Negative Power Supply.** -9 Volts. A 0.1μF decoupling capacitor must be connected across GND and VEE as close to the device as possible.

3.0 FUNCTIONAL DESCRIPTIONS

3.1. Transmission Path

The transmission data is input from TX+/- pins differentially. In general, this differential signal is coupled through an AUI isolation transformer. In the MAU design, it is preferable that an equivalent 78 Ohm load be placed across these 2 pins for proper loading for the signal source. Improper load termination may cause excess undershoot at the end of the packet, which causes the dribble bit to be transmitted erroneously.

The transmission signal is first checked against the on-chip DC/AC squelch condition. If the signal is greater than the squelch threshold (-175 to -300 mV) and the width is wider than 17 nsec, the squelch is turned off. The squelch remains off until the DC squelch condition is not met or an end-of-packet IDL is detected (at the end of the packet, data remains at 1 for longer than 175 nsec). Once IDL is detected, MTD492 provides a 0.8 usec rejection window that prevents dribble bit transmission at the AUI interface.

When the squelch is off, the transmission path is enabled and data is fed into a waveform shaping circuit followed by the transmission output buffer. The waveform shaping function controls the output rise/fall time between 20nsec and 30 nsec, and minimizes the mismatch between the rise/fall time. MTD492 provides a current source output that should be connected to the coaxial cable through at least one isolation diode. When data is high, the output current is virtually zero (there is approximately less than 1mA output in this state to maintain the linearity of the output buffer); when data is low, the output current peaks at around 80 mA. This provides an approximate 2V peak to peak swing on a 25 Ohm load. Due to the nature of Manchester code, the average output DC current is half of the peak - 40 mA, i.e. 1V DC average on the cable 25 Ohm load.

3.2. Reception Path

The signal on the coaxial cable is first buffered. The DC average of the signal is extracted by a low pass filter. When the DC average exceeds the carrier sense threshold (Vcs), the reception data path is turned on. The signal goes through a high pass filter for equalization of high frequency loss on the cable and then is compared with its center value. The comparator output is amplified by the AUI driver to provide adequate driving for the RX+/- output.

The end of the packet is determined by 2 conditions. If the received data is high longer than 175nsec or the DC average does not meet the carrier sense threshold, the reception data path is turned off. MTD492 then appends the IDL pulse to the end of the packet. A rejection window of 1 usec that blocks the data reception path is also turned on.

The RX+/- output pin is driven by a source follower. Therefore, an external pull-down load is required for these 2 pins. During idle state, RX+/- is biased at around -1.5V.

3.3. Collision Detection Path

In 10Base2 and 10Base5, a collision condition is determined by the DC level on the cable. The DC average is extracted by a low pass filter. The output of the filter is compared with an internally set threshold (Vcd) to determine the collision condition. The internal threshold is set for the reception-collision mode. By definition, MTD492 will detect collision conditions caused by more than 2 stations simultaneously transmitting.

The collision detection threshold can be shifted by applying a voltage to the CDS pin. This is typically done by a resistor divider network between GND and VEE to implement the transmission-collision mode detection. Transmission-collision differs from reception-collision in that transmission-collision will only detect a 2-station collision if it is transmitting.

Once a collision is detected, MTD492 turns on the CD+/- pins. These 2 pins are also driven by source followers, thus requiring external pull-down resistors. However, the followers are disabled during idle time, and CD+/- will be pulled down to VEE and no current will flow through the external resistors.

Because Vcd is always larger than Vcs, when a collision occurs the reception path will also be turned on. MTD492 implements an internal timer of 250 msec to detect the extended collision period. When a collision condition period extends beyond this timer, the reception path is turned off. Any interruption of the collision will reset the timer.

3.4. Reference and Control

The internal reference of MTD492 is generated by an on-chip bandgap circuit. An external resistor connected between RR+ and RR- pins is used to set the reference current level. Typically, a precision 1K Ohm resistor should be used. RR+ is internally shorted to GND, while RR- is biased at around -1.25V.

The heartbeat and jabber functions of MTD492 are implemented in the transmission state machine. The heartbeat function is controlled by the HBE pin. MTD492 also provides a test mode that disables the jabber function also controlled by the HBE pin. HBE has a 3-level input. It is biased internally at around -4.5V (0.5Vee). When HBE is pulled high by a low value resistor (<4.7K), the heartbeat function is enabled; when it is pulled low, the heartbeat is disabled. If it is driven to the mid-level or left floating, the jabber is disabled. The exit of the jabber disable state takes about 0.5 sec (jabber reset time).

4.0 ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage(VEE)	-12V
Input Voltage	GND+0.3 to VEE-0.3V
Storage Temperature	-65° to 150°C
Ambient Operating Temperature	0° to 70°C
ESD Protection except for Pin14	2000V

5.0 ELECTRICAL CHARACTERISTICS (under operating conditions) (Note 1)

OPERATING CONDITIONS

DC Supply Voltage (VEE) 8.55-9.45V
Operating Temperature 0° to 70°C

Parameter	Symbol	Min	Typ	Max	Unit
Recommended Supply Voltage	VEE	-8.55	-9.0	-9.45	V
Supply Current (all VEE pins) Non-transmission	IEEidle	-	-25	-35	mA
Transmission	IEExmt	-	-70	-80	mA
Receiver Input Bias Current (RXI)	Irxi	-2	-	+25	μA
Transmission Output DC Current (TXO)	Itdc	37	41	45	mA
Transmission Output AC Current (TXO)	Itac	±28	-	Itdc	mA
Collision Threshold (Reception Mode)	Vcd	-1.45	-1.53	-1.62	V
Carrier Sense Threshold (RXI)	Vcs	-0.38	-0.45	-0.52	V
Differential Output Voltage (RX±,CD±)	Vod	±500	-	±1500	mV
DC Common Mode Output Voltage (RX±)	Vocrx	-1.0	-2.0	-3.0	V
DC Common Mode Output Voltage (CD±) (Note 2)	Voccd	VEE	VEE	VEE	V
Idle State Differential Offset Voltage(RX±,CD±)	Vob	-	0	±40	mV
Transmission Squelch Threshold(TX±) (Note 3)	Vts	-175	-225	-300	mV
Input Capacitance (RXI)	Cx	-	1.5	-	pF
Shunt Resistance - Non-transmission	Rrxi	100	-	-	kΩ
Shunt Resistance - Transmission	Rtxo	10	-	-	kΩ

Notes: 1. Testing is done under the testing load defined in Figure 6.
2. During an idle condition, Voc is pulled down to VEE to minimize the power dissipation across the load resistors connected to CD±pins.
3. Tested under continuous 5MHz waveform that represents the preamble.

6.0 SWITCHING CHARACTERISTICS (under operating conditions) (Note 1)

Parameter	Symbol	Min	Typ	Max	Unit
Reception Start-up Delay (RXI to RX±)	Tron	-	2.5	5	bits
Reception Propagation Delay (RXI to RX±)	Trd	-	35	50	ns
Differential Output Rise Time (RX±,CD±)	Trr	-	4	7	ns
Differential Output Fall Time (RX±,CD±)	Trf	-	4	7	ns
Receiver and Cable Total Jitter	Trj	-	±2	-	ns
Transmission Start-up Delay	Ttst	-	1	2	bits
Transmission Propagation Delay	Ttd	-	25	50	ns
Transmission Rise Time (10%-90%) (TXO)	Ttr	20	25	30	ns
Transmission Fall Time (10%-90%) (TXO)	Ttf	20	25	30	ns
Ttr and Trf Mismatch	Ttm	-	±0.5	±3.0	ns
Transmission Skew(TXO)	Tts	-	±0.5	±2	ns
Transmission Turn-on Pulse Width at Vts(TX+) (Note 4)	Tton	10	20	40	ns
Transmission Turn-off Delay	Ttoff	130	200	260	ns
Transmission IDL Detection Time (Note 5)	Ttidl	130	170	200	ns
Collision Turn-on Delay	Tcon	-	7	13	bits
Collision Turn-off Delay	Tcoff	-	-	20	bits

Collision Frequency (CD±)	Fcp	8.5	10	12.5	MHz
Collision Pulse Width (CD±)	Tcp	40	50	60	ns
Extended Collision Detection Time (Note 6)	Tcxd	100	200	300	ms
CD Heartbeat Delay (TX± to CD±)	Thon	0.6	1.1	1.6	µs
CD Heartbeat Duration(CD±)	Thw	0.5	1.0	1.5	µs
Jabber Activation Delay(TX± to CD±)	Tja	20	26	32	ms
Jabber Reset Time-out (TX± to TXO and CD±)	Tjr	300	420	550	ms

Notes: 4. For a minimum pulse amplitude of ≥ -300 mV.
5. IDL detection precedes the transmission turn-off by transmission propagation delay.
6. Time needed to detect an extended period of collision in order to turn off the reception path.

7.0 TIMING DIAGRAM

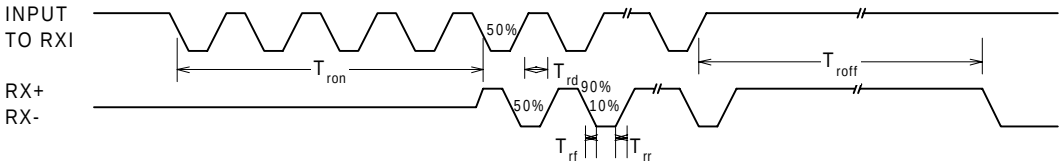


Figure 1. Reception Timing

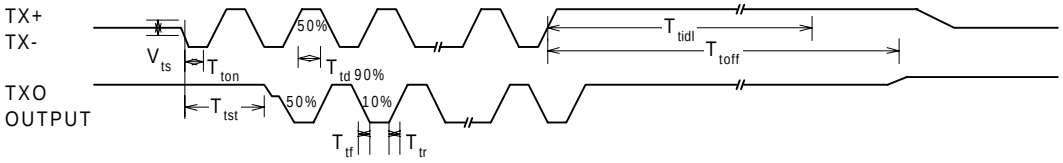


Figure 2. Transmission Timing

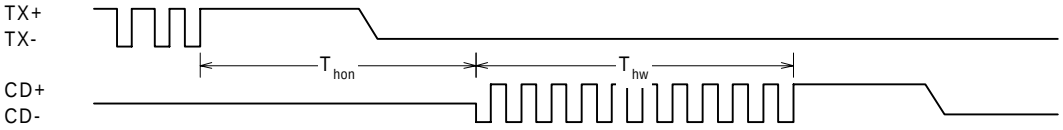


Figure 3. Heartbeat Timing

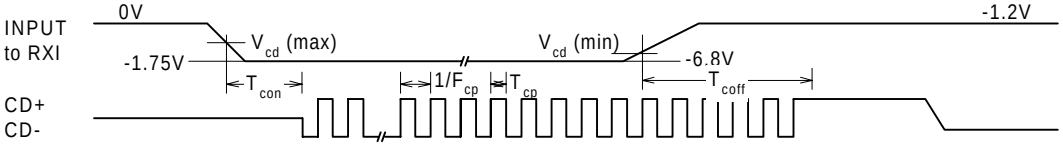


Figure 4. Collision Timing

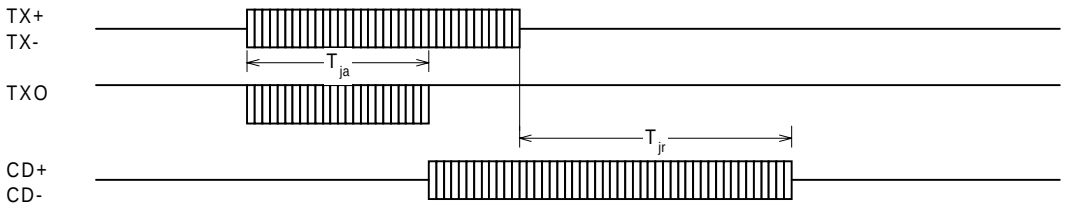
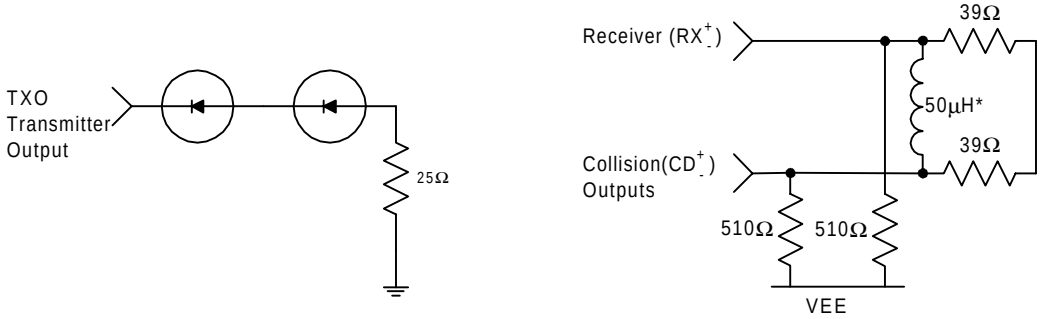


Figure 5. Jabber Timing



*: 50μH inductor is used for testing purposes. Pulse transformers with higher primary inductance are recommended.

Figure 6. Test Loads

8.0 PACKAGE DIMENSION